

ACCESS FREE VERILOG CODING FOR LOGIC SYNTHESIS

Verilog [x]rights to Gateway's Verilog and the Verilog-XL, the HDL-simulator that would become the de facto standard (of Verilog logic simulators) for the next decade... SystemVerilog [x]to Verilog's "reg" type: logic [31:0] my_var; Verilog-1995 and -2001 limit reg variables to behavioral statements such as RTL code. SystemVerilog extends... High-level synthesis [x]Logic synthesis High-level verification (HLV) SystemVerilog Hardware acceleration Coussy, Philippe; Morawiec, Adam, eds. (2008). High-Level Synthesis... Hardware description language (category Logic design) [x]integration with a logic simulator was one of the few ways to use object-oriented programming in hardware verification. System Verilog is the first major... VHDL [x]attractive that logic simulators were developed that could read the VHDL files. The next step was the development of logic synthesis tools that read the... Field-programmable gate array (redirect from Field programmable logic array) [x]description in VHDL or Verilog is simulated by creating test benches to simulate the system and observe results. Then, after the synthesis engine has mapped... Verilog-to-Routing [x]main component applications: ODIN II which compiles Verilog code to a circuit in Berkeley Logic Interchange Format (BLIF), a human-readable graph representation... Arithmetic logic unit [x]description written in VHDL, Verilog or some other hardware description language. For example, the following VHDL code describes a very simple 8-bit... List of HDL simulators (redirect from List of Verilog Simulators) [x]written in one of the hardware description languages, such as VHDL, Verilog, SystemVerilog. This page is intended to list current and historical HDL simulators... Logic simulation [x]Tsu-Hua and Tan, Chong Guan (1995). Practical code coverage for Verilog. 1995 IEEE International Verilog HDL Conference. IEEE. pp. 99–104.{{cite conference}}:... Bluespec (redirect from Bluespec SystemVerilog) [x]designers and architects. Bluespec supplies high-level synthesis (electronic system-level (ESL) logic synthesis) with register-transfer level (RTL). The first... Electronic design automation [x]description (e.g. written in Verilog or VHDL) into a discrete netlist or representation of logic gates. Schematic capture – For standard cell digital, analog... C to HDL (redirect from C to Verilog compiler) [x]language or C-like computer code into a hardware description language (HDL) such as VHDL or Verilog. The converted code can then be synthesized and translated... High-level verification [x](RTL) abstract level. For high-level synthesis (HLS or C synthesis), HLV is to HLS as functional verification is to logic synthesis. Electronic digital... Comparison of EDA software (section Free & open source software for high-level synthesis) [x]high-level synthesis software is used to edit and verify code written in one of the mainstream hardware description languages (HDL) like VHDL or Verilog. Other... ARM11 [x]execution and data transfers. ARM makes an effort to promote recommended Verilog coding styles and techniques. This ensures semantically rigorous designs, preserving... Semiconductor intellectual property core (redirect from Logic core) [x]offered as synthesizable RTL in a hardware description language such as Verilog or VHDL. These are analogous to low-level languages such as C in the field... Karnaugh map (redirect from Reflection map (logic optimization)) [x](November 1953) [1953-04-23, 1953-03-17]. "The Map Method for Synthesis of Combinational Logic Circuits" (PDF). Transactions of the American Institute of... Formal verification (category Logic in computer science) [x]temporal logics, such as linear temporal logic (LTL), Property Specification Language (PSL), SystemVerilog Assertions (SVA), or computational tree logic (CTL)... Don't-care term (redirect from Don't-care (logic)) [x]unknown value in a multi-valued logic system, in which case it may also be called an X value or don't know. In the Verilog hardware description language...

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